Remarks

Claim Objections

Claims 3, 9, 24 and 30 were objected to on grounds that it is unclear how "a common layer" and "a dielectric layer" are interconnected and associated with the input/output line. In the context of these claims, the "common layer" on which the driver and receiver circuits are implemented is illustrated as semiconductor layer 28 in Figs. 5-7, while the "separate layer" in which the T-coil circuit inductors are implemented is illustrated as metallization layer 32, which interconnects desired portions of the underlying circuit layer by means of vias 34 that extend through the dielectric layer 30 to the circuit layer 28 (see specification page 9, lines 4-16). The input/output line for this embodiment could be connected to the driver/receiver circuitry by a flip-chip "bump" 44 that connects to metallization layer 32 and from there to the circuit layer 28 as illustrated in Figs. 5 and 6, by a wire bond connection 52 to a bonding pad on the metallization layer 32, as illustrated in Fig. 7 (page 10, lines 26-31), or by any other convenient connection mechanism. In any case, the electrical connection is between the input/output line and the common layer, with the T-coil circuit on the separate layer connected to the IC on the common layer by electrical interconnects (vias 34 in illustrative Figs. 5-7) that extend through the dielectric layer. Claims 3, 9, 24 and 30 have been amended accordingly to require (1) that the driver and receiver circuits are implemented on a common layer of an integrated circuit "to which said input/output line is connected", and

(2) "electrical interconnects extending through said dielectric layer between said T-coil circuit and said IC".

In claims 4, 10, 25 and 31 it was found to be unclear how the flip-chip bump is interconnected with the T-coil. Actually, there is no requirement that the T-coil be connected to the flip-chip bump at all. As described at page 10, lines 8-25, the flip-chip bump is provided to connect "the circuitry to an additional IC chip by means of a conventional flip-chip bump 44". This connection is accomplished, as illustrated in Figs. 5 and 6, from the flip-chip bump 44 through its associated redistribution layer 46, and then through via(s) 48 between the redistribution layer 46 and the metallization layer 32 that provides interconnects between desired portions of the underlined circuit layer 28 (see page 9, lines 4-23). It would be possible to connect the flip-chip bump directly to the T-coil inductors in this way, but there is no requirement that this be done. Accordingly, to further specify the relationship between the flip-chip bump and the remainder of the circuitry, claims 4, 10, 25 and 31 have been amended to require that the redistribution layer associated with the flip-chip bump be "connected to a metallization layer that also provides interconnects for said driver and receiver circuits, and connects said T-coil circuit to said driver and receiver circuits".

Claims 5-6 and 26-27 were objected to as being dependent upon a rejected base claim, but were found to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 5 and 26 have been rewritten accordingly,

while claims 6 and 27 depend respectively from rewritten claims 5 and 26.

Claim 7 has been corrected by deleting an unnecessary comma in the first line.

Invention Predating Reference

Patent No. 6,463,395 to Iorga, upon which all of the prior art rejection were based, was applied for on December 9, 1999. (It is assumed there was a typographical error in the patent number given in the Office action; the correct patent number is 4,463,395.)

The Declaration of Co-Inventor Robert A. Duris submitted with the Response to December 1, 2005 Office Action established diligence, beginning not later than April 13, 2000, in physically reducing the invention to practice. The enclosed Declaration of Robert A. Duris establishes an earlier reduction of the invention to practice on November 30, 1999 by means of a circuit simulation and testing thereof. The enclosed Declaration of Bruce Hecht, another co-inventor, coupled with the previous Duris declaration, establishes diligence in physically reducing the invention to practice in the form of a working chip beginning not later than September 20, 1999. Both the simulation reduction to practice, and the beginning of diligence towards a physical reduction to practice, occurred prior to the Iorga '395 filing date.

The enclosed Declaration of Robert A. Duris establishes that a circuit embodying the independent claims of the application was simulated on November 30, 1999. The simulation tests "demonstrate that the simulated circuit with a single T-coil successfully compensated for

increasing levels of parasitic capacitance in the receiver circuit…" (Duris para. 5). The reliability of the simulation in predicting physical circuit operation was established by testing wafers that included the simulation circuit but had two T-coils each, rather than the single T-coil of the simulation. The physical wafers were received on October 12, 2000 and tested on October 17, 2000. For comparison, a similar circuit but without the T-coils was also tested on October 18, 2000. The tests indicated that "the addition of the post-passivation T-coils was successful in substantially compensating the receiver circuit capacitance." (Duris Declaration para. 6).

Exhibit 8 of the enclosed Declaration of Bruce Hecht is a copy of a Project Schedule dated July 15, 2000 for the product that incorporated the subject matter of the present patent application. The Project Schedule shows that, as of July 12, 2000, the project had been worked on for continuous periods of time from September 20, 1999 through May 26, 2000, and that as of the latter date additional tasks were regularly scheduled to bring the project to completion. The project had a scheduled conclusion on September 1, 2000 with an evaluation of incorporating the invention by Agilent, a customer for other products. Based upon Agilent's feedback, extensive modifications to the product design were made. (Hecht para. 12). As of July 12, 2000, the following tasks had been accomplished beginning September 20, 1999:

- Driver Design 9/27/99-3/3/00.
- Formatter Design 9/20/99-2/10/00.
- Miscellaneous Cells 1/3/00-1/24/00.
- Comparator Design 9/20/99-12/10/99.

- AB Driver Design 9/20/99-2/15/00.
- Top Level 1/19/00-2/25/00.
- Design Review 2/28/00.
- Layout Review 2/29/00.
- Top Level Simulations 3/1/00-3/23/00.
- Power reduction design (Logic, IO, Comp Pwr Dn) 3/24/00-3/28/00.
- Final pwr reduction/top level layout 3/29/00-4/20/00.
- Final top level simulations 4/21/00-4/27/00.
- Final Design Review 4/28/00.
- Tape out 5/1/00-5/28/00.
- Wafer Fab (50% complete) 5/29/00-7/12/00.

Coupled with the Duris declaration accompanying the Response to December 1, 2005 Office action, the enclosed Hecht declaration establishes an almost continuous effort, with only minor interruptions, to physically reduce the invention to practice in an integrated circuit chip from September 20, 1999 to the actual reduction to practice in October 2000. Since Patent No. 6,463,395 to Iorga, which was relied upon in the September 5, 2006 Office action, had a filing date of December 10, 1999, this reference is accordingly not prior art to the present invention under 35 U.S.C. 102(e). The reduction of the present invention to practice through the circuit simulation on November 30, 1999 independently removes Iorga '395 as prior art under 35 U.S.C. 102(e).

Patentable Distinctions over Iorga '395

Claims 1-2, 7, 9, 22-23 and 28-29 were rejected under 35 U.S.C. 102(e) as anticipated by Iorga Patent No. 6,462,395. Claims 3, 8, 24 and 30 were rejected under 35 U.S.C. 103(a) over the same Iorga reference.

New claims 32-39 presented herein include an important distinguishing feature over Iorga '395. These claims and the accompanying remarks are presented in case, even though the Iorga '395 patent is not prior art to the present invention under 35 U.S.C. 102(e), its subject matter has become prior art through some other means unknown to applicants.

In Iorga '395 the two inductors 96, 97 cited in the Office action are not mutually coupled ("96" and "97" appear to be typographical errors; the inductive elements cited in Iorga Fig. 7 are 97 and 99). Nor are inductors 27, 29 in Iorga Fig. 2 mutually coupled. Actually, elements 97 and 99 in Fig. 7 represent the inductances of signal lead branches 91 and 93, respectively, in Fig. 6 (see column 6, lines 1-15). Similarly, inductor elements 27 and 29 in Fig. 2 represent the inductances of signal lead branches 21 and 23 in Fig. 1 (column 3, lines 29-45). There is no disclosure of any coupling between these elements, nor are the dot symbols that are conventionally used to indicate mutual coupling between inductors (as in Figs. 1-3 of the present application) used in Iorga '395.

While inductors without mutual coupling will provide some benefit in compensating for the receiver capacitance in the present invention, the use of mutually coupled inductors as in the preferred T-coil implementation of the invention provides substantially greater benefits. The mutual coupling between inductors L1 and L2 in the present application is explicitly disclosed in the specification: "These inductors are also coupled to one another by some degree of mutual inductance." (page 6, lines 1-2); "As indicated by the dotting convention used in the figures,

the individual coils of each T-coil circuit are connected in series. The coils are also fabricated in proximity to each other so that they mutually couple." (page 7, lines 3-6).

The enclosed Hecht declaration confirms his understanding that inductances 97, 99 and 27, 29 in Iorga '395 are not coupled to each other (Hecht para. 3). The declaration goes on to demonstrate the improved performance of coupled inductors compared to uncoupled ones. Paragraphs 4-9 describe simulations which Mr. Hecht performed to compare the effectiveness of uncoupled vs. coupled inductors in compensating for a load capacitance of 1pF, with a 500mV input. The circuits he compared included (1) no compensation, (2) a pair of uncoupled compensation inductors on either side of the capacitive load, as in Iorga '395, (3) a pair of coupled inductors on either side of the load capacitor, connected as a T-coil with a coupling factor of 0.5, and (4) the addition of a bridging capacitor to the T-coil. The results showed some compensation for the uncoupled compensation inductors, a notably improved compensation for the coupled inductors, and even better compensation with a bridging capacitor for the T-coil.

Mr. Hecht also simulated and compared the Iorga '395 circuit shown in Fig. 5 of Iorga '395, the T-coil circuit illustrated in Fig. 1 of the present patent application, but without the bridge capacitor Cb1, and the T-coil circuit of present Fig. 1 with the bridge capacitor. The simulations were performed with the same values of compensating inductors as for the simulated circuits in his Exhibit 1, and the results were similar. "Thus, the use of

mutually coupled inductors was found to both enable the elimination of negative bumps present with the Iorga circuit, and to reduce the maximum voltage excursion, with a bridge capacitor further improving the load capacitance compensation." (para. 10). A negative reflection "bump" is explained in paragragh 6 of the declaration as generally being less desirable than a positive bump because it can cause false triggering in an automatic test equipment system.

New independent claims 32, 34, 36 and 38 have been added, modeled respectively on claims 1, 7, 22 and 28, but adding a requirement for "said matching network comprising a plurality of inductors with mutual inductive coupling". New dependent claims 33, 35, 37 and 39 specify that the passive matching network of their respective parent claims 32, 34, 36 and 38 comprises a T-coil circuit. The requirement for mutual inductive coupling between the compensating inductors makes the new claims patentable even if the subject matter of Iorga '395 has entered the prior art through some means other than the patent itself.

In view of the above amendment and remarks, a Notice of Allowance is respectfully requested.

Respectfully submitted,

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